Remarks

The above-referenced application has been reviewed in light of the Examiner's Office Action dated June 11, 2004. The Examiner's indication of allowable subject matter is gratefully acknowledged. Claims 4, 10, 20, 26 and 30 have been amended. Therefore, Claims 1-30 are currently pending in this application.

In accordance with the Office Action, the drawings stand objected to under 37 C.F.R. 1.83(a) for failing to show the "second circuit" of Claims 1, 8, 11, 18, 21 and 28. Applicant traverses. The application as originally filed includes a Figure 4, as described at page 8, line 18 through page 9, line 3. The circuit of Figure 4 provides an output "for charging ... a pumping voltage" (spec. at 8, line 19). The "second circuit" of Claim 1, for example, recites, *inter alia*, "a second circuit ... for generating a pumping voltage". Accordingly, the "second circuit" is adequately shown and described in the application, as filed, such that one of ordinary skill in the pertinent art could practice the invention in accordance with the teachings therein, without the need for undue experimentation.

In accordance with the Office Action, Figures 1 and 2 stand objected to under MPEP 608.02(g) for failure to recite a legend indicative of prior art. Proposed replacement sheets showing Figures 1 and 2 are respectfully submitted herewith, each indicating the legend "Prior Art".

In accordance with the Office Action, the specification stands objected to for informalities at page 10, line 12, as compared with Figure 7. Accordingly, the

specification has been corrected to accurately describe the drawing of Figure 7, as originally filed. No new matter has been added.

In accordance with the Office Action, Claims 1-30 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 4, 10, 20, 26 and 30 have been amended. Applicant respectfully submits that Claims 1-30 do particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Applicant respectfully traverses with respect to Claims 1, 11 and 21. Claim 1 recites:

> 1. A flash memory comprising:
>
> a memory cell array having pages, each of the pages including memory cells, bit lines and source lines;
>
> a first circuit in signal communication with the bit lines for charging non-selected bit lines among the bit lines to a first voltage level at a first time;
>
> a second circuit in signal communication with the bit lines for generating a pumping voltage higher than a power supply voltage at a second time; and
>
> a third circuit in signal communication with the bit lines for charging the bit lines to a second voltage level at a third time.

Here, the unqualified term "bit lines" unambiguously refers to all bit lines in each of the first, second, third and fourth clauses. The second clause recites, *inter alia*, "non-selected bit lines among the bit lines". Thus, the qualified term "non-selected bit lines" comprises a subset of "the bit lines". This introduction of the qualified term "non-selected bit lines" leaves undisturbed the original term "bit lines" by reciting the limitation "among the bit lines". Accordingly, it is clear on its face that the recitation "charging the bit lines to a second voltage level" at lines 8-9 refers to all of "the bit lines", inclusive of the "non-selected bitlines". This is further supported by the specification at page 11, line 7, which describes as follows:

> "According to exemplary embodiments of the present invention, the non-selected bit lines are first charged to a predetermined voltage level [VDD – Vtn] (at t1). Then, the high voltage required for the program operation is generated (at tp). After a predetermined interval elapses, the selected bit line is precharged together with the previously charged non-selected bit lines (at t2)."

Claims 11 and 21 recite limitations similar to Claim 1 and are likewise in compliance with 35 U.S.C. 112, second paragraph.

Amended Claim 4 recites, *inter alia*, "the second time is later than the first time by a predetermined interval". Amended Claim 4 is believed to overcome the Examiner's rejection.

Amended Claim 10 recites, *inter alia*, "wherein the third circuit charges the bit lines to the second voltage". Amended Claim 10 is believed to overcome the Examiner's rejection.

Amended Claim 20 recites, *inter alia*, "wherein the third circuit charges the bit lines to the second voltage". Amended Claim 20 is believed to overcome the Examiner's rejection.

Amended Claim 26 recites, *inter alia*, "wherein the first circuit is responsive to a high voltage signal and the address bit". Amended Claim 26 is believed to overcome the Examiner's rejection.

Amended Claim 30 recites, *inter alia*, "wherein the third circuit activates at least one precharge signal for a grouped memory cell array according to the logic state of the address bit, the at least one precharge signal being responsive to a program start signal at the third time." Amended Claim 30 is believed to overcome the Examiner's rejection.

Therefore, Applicant respectfully submits that Claims 1-30 do particularly point out and distinctly claim the subject matter which Applicant regards as the invention, and are therefore in compliance with 35 U.S.C. 112, second paragraph. The Examiner's indication that Claims 1-30 would be allowable if the above-addressed rejections under 35 U.S.C. 112, second paragraph were overcome is gratefully acknowledged.

Conclusion

Accordingly, it is respectfully submitted that independent Claims 1, 11 and 21 are in condition for allowance for at least the reasons stated above. Since Claims 2-10, 12-20 and 22-30 each depend from one of the above claims and necessarily include each of the elements and limitations thereof, it is respectfully submitted that these claims are also in condition for allowance for at least the reasons stated, and for reciting additional patentable subject matter. Thus, each of Claims 1-30 is in condition for allowance. All issues raised by the Examiner having been addressed, reconsideration of the rejections and an early and favorable allowance of this case is earnestly solicited.

Respectfully Submitted,

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In the Drawings:

Please substitute the attached replacement sheets showing Figures 1 and 2.